WNMD2196A

Dual N-Channel, 12V, 19A, Power MOSFET

https://www.omnivision-group.com

V_{SSS} (V)	Max $R_{SS(on)}$ (mΩ)
12	1.5@ V_{GS}=4.5V
	1.7@ V_{GS} =3.8V
	2.6@ V_{GS}=3.1V
	4.0@ V_{GS}=2.5V
ESD Rating:2000V HBM	

Descriptions

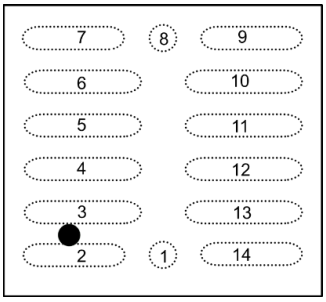
The WNMD2196A is Dual N-Channel enhancement MOS Field Effect Transistor and connecting the Drains on the circuit board is not required because the Drains of the MOSFET1 and the MOSFET2 are internally connected. Uses advanced trench technology and design to provide excellent $R_{SS(ON)}$ with low gate charge. This device is designed for Lithium-Ion battery protection circuit. The WNMD2196A is available in CSP-14L package. Standard Product WNMD2196A is Pb-free and Halogen-free.

Features

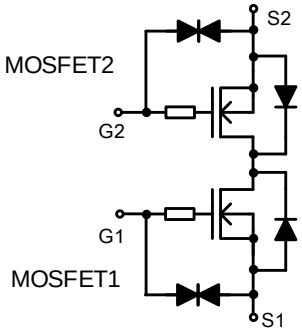
- Trench Technology
- Supper high density cell design
- Excellent ON resistance for higher DC current
- Extremely Low Threshold Voltage
- Common-drain type
- Small package CSP-14L

Applications

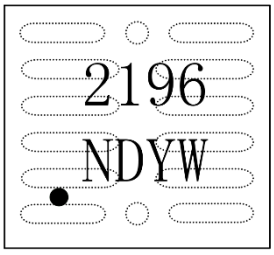
- Lithium-Ion battery protection circuit



Gate1 (FET1) = 1
Source1 (FET1) = 2,3,4,5,6,7
Gate2 (FET2) = 8
Source2 (FET2) = 9,10,11,12,13,14
CSP-14L (Top view)



Pin Configuration



2196 = Device Code
ND = Special Code
Y = Year
W = Week
Marking

Order information

Device	Package	Shipping
WNMD2196A-14/TR	CSP-14L	3000/Reel&Tape

Absolute Maximum ratings

Parameter		Symbol	Maximum	Unit
Source -Source Voltage		V_{SS}	12	V
Gate-Source Voltage		V_{GS}	±8	
Continuous Source Current	T_A=25°C	I_S[a]	19	A
		I_S[b]	48	
Pulsed Source Current [c]		I_{SM}	189	
Maximum Power Dissipation	T_A=25°C	P_D[a]	0.57	W
		P_D[b]	3.62	
Operating Junction Temperature		T_J	-55 to 150	°C
Storage Temperature Range		T_{STG}	-55 to 150	°C

Thermal resistance ratings

Single Operation				
Parameter	**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$[a]	146	219	°C/W
	$R_{\theta JA}$[b]	30	35	

Note:

a. FR-4 board (38mm X 38mm X t1.6mm, 70um Copper) minimum pad covered with copper.

b. Ceramic substrate (70 mm X 70 mm X t1.0 mm, 70um Copper) fully covered with copper.

c. Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial T_J =25°C, the maximum allowed junction temperature of 150°C.

d. The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

Electronics Characteristics (T_A=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Source to Source Voltage	V_{SSS}	V_{GS} = 0 V, I_S = 1mA	12			V
Zero Gate Voltage Drain Current	I_{SSS}	V_{SS} =10 V, V_{GS} = 0V TEST CIRCUIT 1			1	uA
Gate Leakage Current	I_{GSS}	V_{SS} = 0 V, V_{GS} = ±8V TEST CIRCUIT 2			±10	uA
		V_{SS} = 0 V, V_{GS} = ±5V TEST CIRCUIT 2			±1	uA
ON CHARACTERISTICS						
Gate to Source Cut-off Voltage	V_{GS}(th)	V_{SS}= 10 V, I_S = 1mA TEST CIRCUIT 3	0.5	0.9	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	V_{GS} = 4.5V, I_S = 9.8A TEST CIRCUIT 4	0.7	1.1	1.5	mΩ
		V_{GS} = 3.8V, I_S = 9.8A TEST CIRCUIT 4	0.75	1.2	1.7	
		V_{GS} = 3.1V, I_S = 9.8A TEST CIRCUIT 4	0.8	1.45	2.6	
		V_{GS} = 2.5V, I_S = 9.8A TEST CIRCUIT 4	0.9	1.95	4.0	
BODY DIODE CHARACTERISTICS						
Body Diode Forward Voltage	$V_{F(S-S)}$	V_{GS} = 0 V, I_F = 9.8A TEST CIRCUIT 7		0.7	1.2	V
SWITCHING CHARACTERISTICS						
Turn-On Delay Time*	td(ON)	V_{GS} = 4.0V, V_{SS}=6.0V, I_S=9.8A, TEST CIRCUIT 5		1.5		us
Rise Time*	tr			4.0		
Turn-Off Delay Time*	td(OFF)			6.5		
Fall Time*	tf			6.7		
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance*	C_{ISS}	V_{GS} = 0 V, f = 1kHz, V_{SS} = 10 V		5989		pF
Output Capacitance*	C_{OSS}			1200		
Reverse Transfer Capacitance*	C_{RSS}			927		
Total Gate Charge*	$Q_{G(TOT)}$	V_{G1S1} = 4.0 V, V_{SS} = 6.0V, I_S =9.8A TEST CIRCUIT 6		62		nC
Threshold Gate Charge*	$Q_{G(TH)}$			6		
Gate-to-Source Charge*	Q_{GS}			14		
Gate-to-Drain Charge*	Q_{GD}			21		

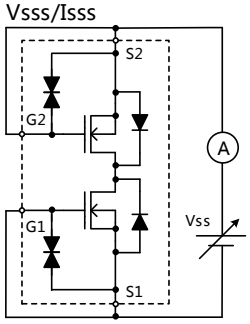
Note:

* Guaranteed by design, not subject to production testing

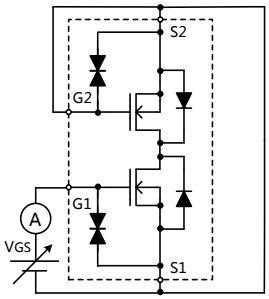
Test Circuit

FET1 and the FET2 are both measured. Test circuits are example of measuring the FET1 side

Test Circuit 1
Vsss/Isss



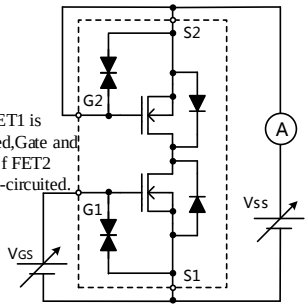
Test Circuit 2
IGSS



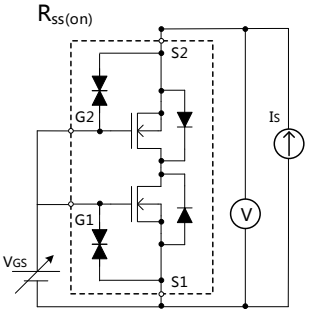
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
VGS(th)

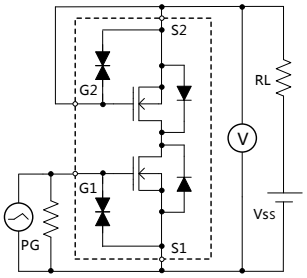
When FET1 is measured,Gate and Source of FET2 are short-circuited.



Test Circuit 4
Rss(on)

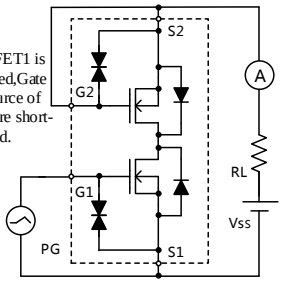


Test Circuit 5
td(on), tr, td(off), tf

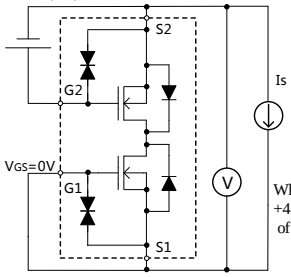


Test Circuit 6
Qg

When FET1 is measured,Gate and Source of FET2 are short-circuited.

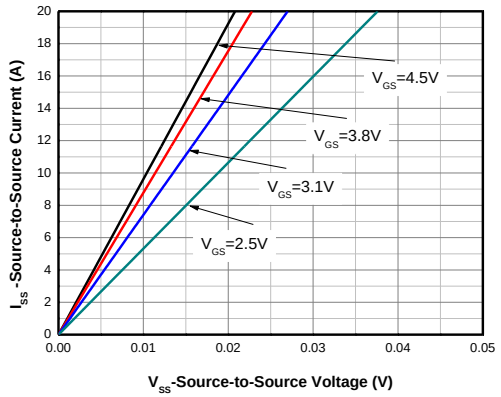


Test Circuit 7
VF(S-S)

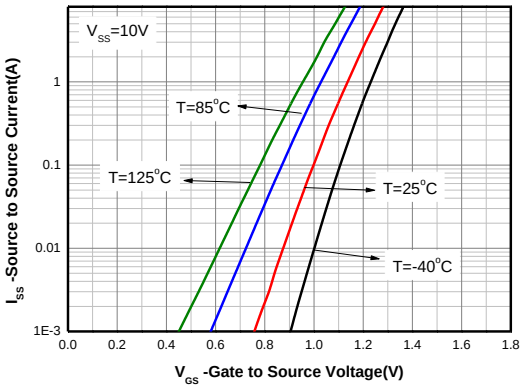


When FET1 is measured, +4.5V is added to V_{GS} of FET2.

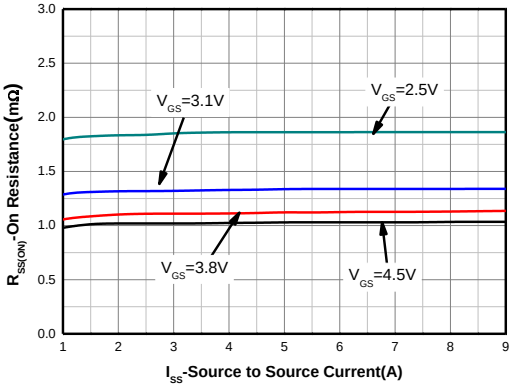
Typical Characteristics (T_A=25°C, unless otherwise noted)



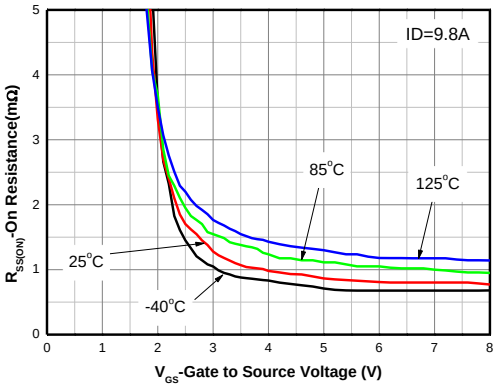
Output Characteristics [d]



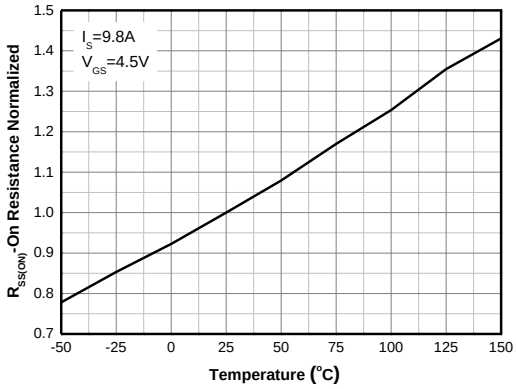
Transfer Characteristics [d]



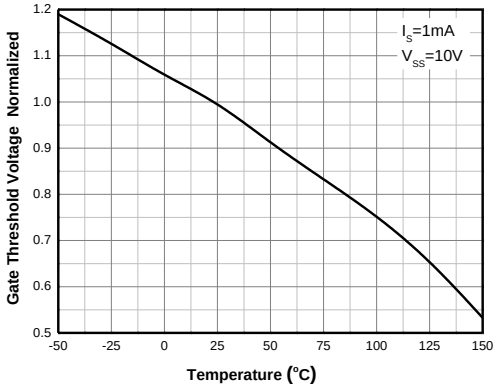
On-Resistance vs. Source Current [d]



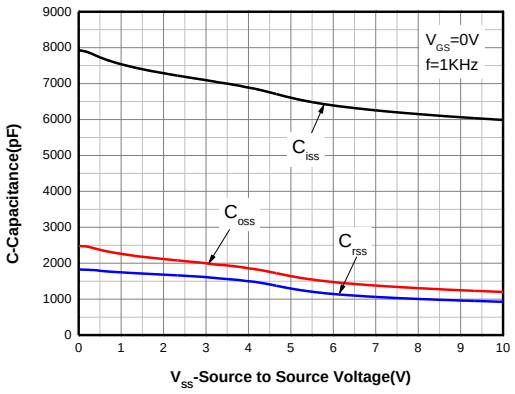
On-Resistance vs. Gate-to-Source Voltage [d]



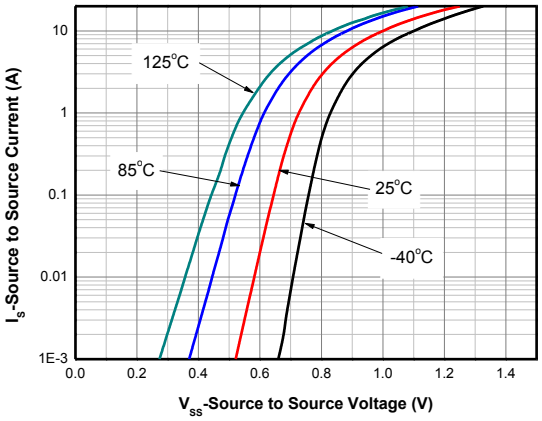
On-Resistance vs. Junction Temperature [d]



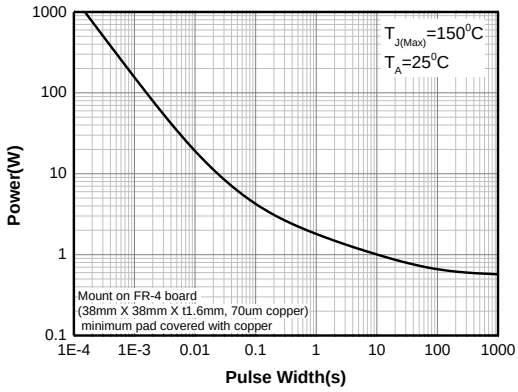
Threshold Voltage vs. Temperature



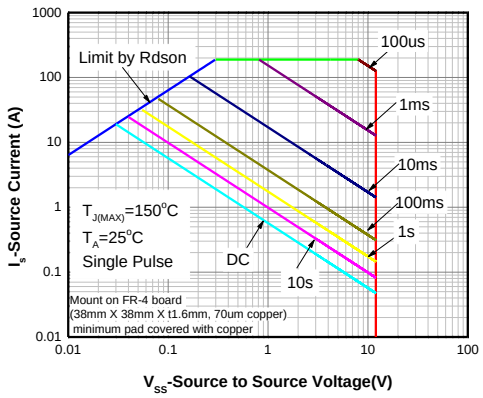
Capacitance



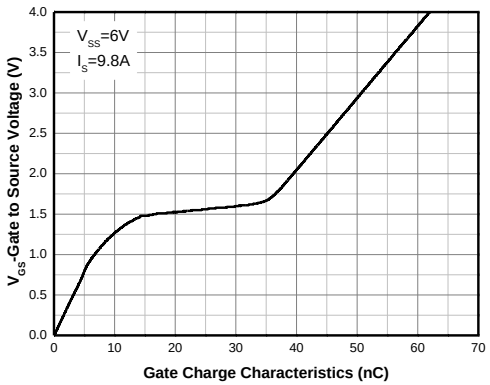
Body Diode Forward Voltage [d]



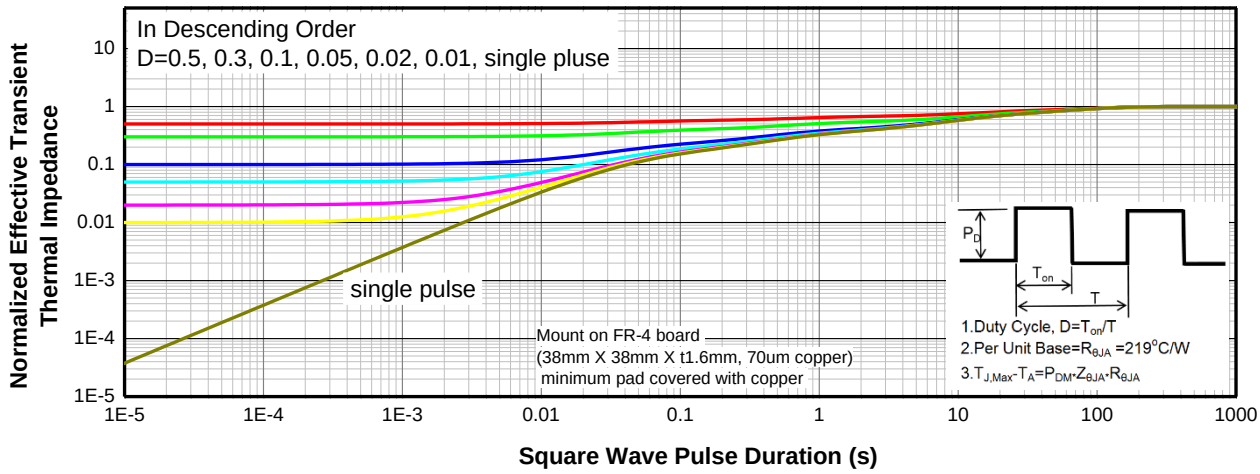
Single Pulse power



Safe Operating Power



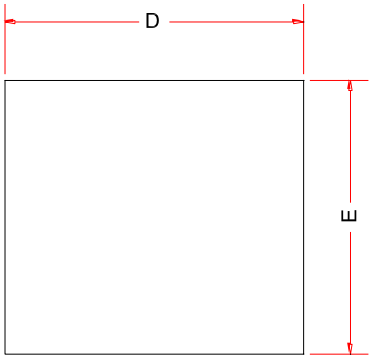
Gate Charge Characteristics



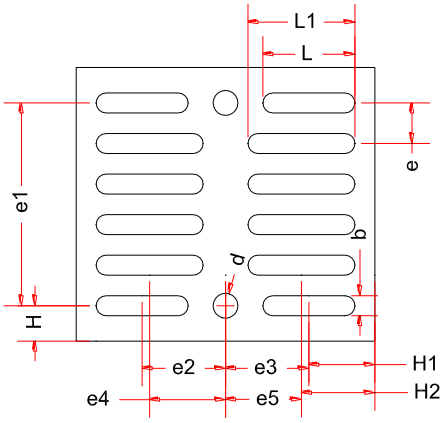
Transient thermal response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS

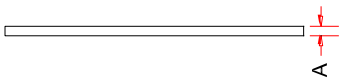
CSP-14L



TOP VIEW



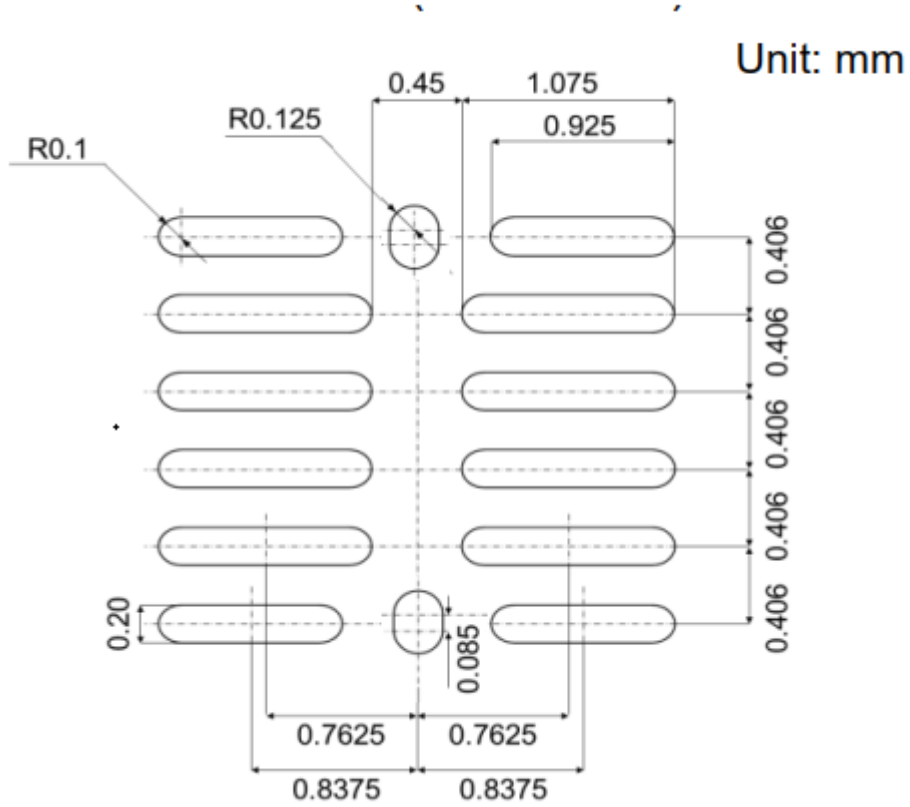
BOTTOM VIEW



SIDE VIEW

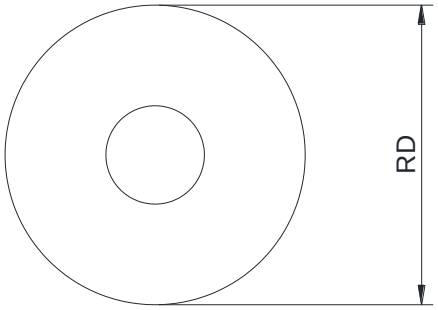
Symbol	Dimensions inMillimeters		
	Min	Typ	Max
A	0.075	0.095	0.125
D	2.96	3.00	3.04
E	2.70	2.74	2.78
b	0.17	0.2	0.23
d		0.25	
e		0.406	
e 1		2.03	
e 2		0.8375	
e 3		0.8375	
e 4		0.7625	
e 5		0.7625	
L	0.922	0.925	0.928
L1	1.072	1.075	1.078
H		0.355	
H1		0.6625	
H2		0.7375	

RECOMMENDED LAND PATTERN (Unit: mm)

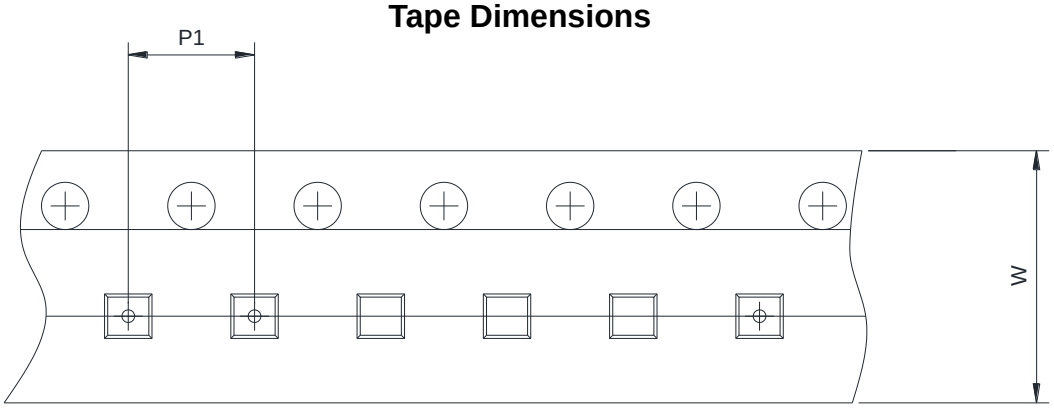


TAPE AND REEL INFORMATION

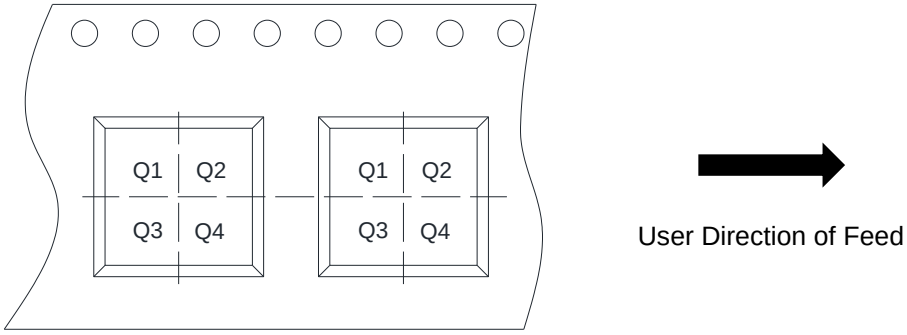
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☐ Q1 ☐ Q2 ☐ Q3 ☑ Q4